AwardBIOS™ Setup for 4.51 Bios

This page lists Setup fields found in the following Setup screens:

- Standard CMOS
- BIOS Features
- Chipset Features
- Power Management
- PNP/PCI Configuration
- Integrated Peripherals

For other setup functions such as setting a password, IDE hard drive detection, saving values, resetting defaults, exiting setup etc., see the appropriate AwardBIOS Setup Guide:

AwardBIOS Setup Manuals
The following are links to Acrobat file versions of various AwardBIOS Setup manuals. If you do not have the Acrobat Reader, you can download it now.

- **AwardBIOS Setup manual for releases prior to August 1996 --** 
  This manual explains Setup options common to all AwardBIOS 4.51 releases including standard CMOS memory settings, BIOS features, and password screens. It also includes descriptions of other Setup functions, such as loading default values and configuring IDE hard drives. Explanations of BIOS POST codes and error messages are also included. Chipset-specific features are not described.
- **AwardBIOS Setup manual for releases after July 1996 -- See table below.** The table below lists manuals that explain specific Setup functionality for newer AwardBIOS products. The table is arranged by BIOS part numbers and chipset names. You can determine the part number of your AwardBIOS by watching the screen after turning on your PC. While the PC's memory is tested you will see the release date, the part number, and other BIOS information at the bottom of the screen. Hint - use the PAUSE key to stop the BIOS software execution. The part number is used to determine the chipset and match it to the correct manual (a lowercase 'x' represents an unimportant character in a part number).

BIOS Part #	Chipset	Manual
2A4KDxxx	ALI 1487/89	
2A5KFxxx	ALI 1521/23	
ALIM6117	ALI M6117	
2A59Fxxx	Intel 82430HX PCIset	
2A59Ixxx	Intel 82430TX PCIset	
2A59Gxxx	Intel 82430VX PCIset	
2A69Kxxx	Intel 82440BX PCIset	
2A69Hxxx	Intel 82440FX PCIset	
2C4UKxxx	OPTi 802G	
2A5UNxxx	OPTi Viper-M (82C556M/7M/8M)	

Numeric A B C D E F G H I J K L M N O P Q R S T U V W XYZ

Numeric	
16 Bit I/O Recovery Time	See 8/16 Bit I/O Recovery Time, below.
16 Bit ISA I/O Command WS	Your system quite possibly has much higher performance than some of your input/output (I/O) devices. This means that unless the system is instructed to allow more time, more wait states, for devices to respond, it might think the device has malfunctioned and stop its request for I/O. If all your I/O devices are capable, then disabling this setting could result in greater throughput. Otherwise, data could be lost.
16 Bit ISA Mem Command WS	When memory is accessed on the ISA bus, the system must allow for the relatively slow speed of the ISA bus. This setting allows you to match the speed of device memory located on the ISA bus with the system ability to read/write to that memory.
1st/2nd Fast	Select up to two DMA channels for Type F DMA, if supported

DMA Channel	by the I/O peripheral using the DMA channel.
1st/2nd/3rd/4th Available IRQ	If an installed PCI device requires interrupt service, you may manually select an unused interrupt line for PCI IRQs. NA indicates the interrupt is assigned to an ISA bus device and is not available to any PCI slot.
2 Bank PBSRAM	For PBSRAMs, 3-1-1-1 timing is available for both read and write transactions at 66 or 75 MHz. VP2
2nd Channel IDE	If you install an add-in IDE interface as the second IDE channel, select Disabled to avoid a conflict with the on-chip second IDE channel.
8/16 Bit I/O Recovery Time	The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is so much faster than the ISA bus. These two fields let you add recovery time (in bus clock cycles) for 16-bit and 8-bit I/O.
A	
ACPI I/O Device Node	Selecting Enabled enables ACPI device node reporting from the BIOS to the operating system. VP2
AGP Aperture Size (MB)	Select the size of the Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation. See www.agpforum.org for AGP information.
ALE During Bus Conversion	Depending on system speed, you can select a Single or a Multiple ALE signal during a bus conversion cycle.
APM BIOS	Select Enabled to turn on the BIOS power-management features.
Asysc. SRAM Read WS	Select the correct cycle timing combination for the system board design and SRAM specifications.
Asysc. SRAM Write WS	Select the correct cycle timing combination for the system board design and SRAM specifications.
AT Clock Option	The system board designer selects whether the AT bus clock is tightly synchronized with the CPU clock or is asynchronous.
AT-BUS Clock	The chipset generates the ISA bus clock (ATCLK) from an

	internal division of PCICLK. You can set the speed of the AT bus in terms of a fraction of the CPU clock speed, or at the fixed speed of 7.16 MHz.
Audio DMA Select	Select a DMA channel for the audio port.
Audio I/O Base Address	Select a base I/O address for the audio port.
Audio IRQ Select	Select an interrupt for the audio port.
Auto Clock Control	If APM is not enabled or not present in your system, the BIOS manages the CPU clock when this field is Enabled in the same way APM power management would manage the clock.
Auto Configuration	Auto Configuration selects predetermined optimal values of chipset parameters. When Disabled, chipset parameters revert to setup information stored in CMOS. Many fields in this screen are not available when Auto Configuration is Enabled.
Auto Detect DIMM/PCI Clk	To reduce the occurrence of electromagnetic interference (EMI), the BIOS detects the presence or absence of components in DIMM and PCI slots and turns off system clock generator pulses to empty slots.
Auto Suspend Timeout	After the selected period of system inactivity, the system enters automatically enters Suspend mode.
B	
Back to Back I/O Delay	Select Enabled to insert three ATCLK signals in back-to-back AT bus I/O cycles.
Bank 0/1 DRAM Type	The value in this field is set by the system board manufacturer, depending on whether the board has paged DRAMs or EDO (extended data output) DRAMs.
BIOS PM on AC	If you wish the BIOS power-management features to remain active when the system is connected to an external power source, set to On.
BIOS PM Timers	After the selected period of inactivity for each subsystem (video, hard drive, peripherals), that subsystem enters Standby mode.
Boot From LAN First	When Enabled, the BIOS attempts to boot from a LAN boot image before it attempts to boot from a local storage device.

Boot Sequence	The original IBM PCs loaded the DOS operating system from drive A (floppy disk), so IBM PC-compatible systems are designed to search for an operating system first on drive A, and then on drive C (hard disk). However, modern computers usually load the operating system from the hard drive, and may even load it from a CD-ROM drive.
Boot Up Floppy Seek	When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360-KB floppy drives have 40 tracks; drives with 720 KB, 1.2 MB, and 1.44 MB capacity all have 80 tracks. Because very few modern PCs have 40-track floppy drives, we recommend that you set this field to Disabled to save time.
Boot Up NumLock Status	Toggle between On or Off to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.
Boot Up System Speed	Select High to boot at the default CPU speed; select Low to boot at the speed of the AT bus. Some add-in peripherals or old software (such as old games) may require a slow CPU speed. The default setting is High.
Burst Write Combining	When this option is Enabled, the chipset assembles long PCI bursts from the data held in these buffers.
Byte Merge	This field controls the byte-merge feature for frame buffer cycles. When Enabled, the controller checks the eight CPU Byte Enable signals to determine if data bytes read from the PCI bus by the CPU can be merged.
Byte Merge Support	Byte merging holds 8- or 16-bit data sent from the CPU to the PCI bus in a buffer where it is accumulated, or merged, into 32-bit data for faster performance. The chipset then writes the data in the buffer to the PCI bus when appropriate. PCI Pipeline and Pipelining combine PCI or CPU pipelining with byte merging. Byte merging is used to enhance video performance.
C	
Cache Read Burst	These SRAM timing numbers are the pattern of cycles the CPU uses to read data from the cache. The system board designer must select the proper combination, depending on the cache size and access speed of the cache SRAMs. Do not reset this option from its default.

Cache Read Wait States	Select the number of wait states for the cache output enable signals. When 0 WS is selected, CROEA# and CROEB# are active for 2 CPU clocks; for 1 WS, CROEA# and CROEB# are active for 3 CPU clocks. The actual number of clocks that CROE# remains active may be longer. The number is automatically adjusted during L2 cache write-back-to-DRAM cycles to synchronize with the DRAM controller.
Cache Timing	For a secondary cache of one bank, select Faster. For a secondary cache of two banks, select Fastest. VP2
Cache Write Burst	Sets the precise timing used during burst writes to the cache.
Cache Write Wait State	The system board designer may elect to insert a wait state into the cache write cycle, if necessary.
CAS Address Hold Time	Select the number of cycles it takes to change the CAS address after CAS has been initiated (asserted) aimed at a target address (location) in DRAM.
CAS Low Time for Write/Read	The number of clocks cycles the CAS signal is pulled low for DRAM writes and reads depends on the DRAM timing. Do not reset this field from the default value specified by the system designer.
CAS# Precharge Time	Select the number of CPU clocks allocated for the CAS# signal to accumulate its charge before the DRAM is refreshed. If insufficient time is allowed, refresh may be incomplete and data lost.
CAS Pulse Width	The system designer must set the duration of a CAS signal pulse (in timer ticks).
Chipset NA# Asserted	Selecting Enabled permits pipelining, in which the chipset signals the CPU for a new memory address before all data transfers for the current cycle are complete, resulting in faster performance.
Chipset Special Features	When disabled, the chipset behaves as if it were the earlier Intel 82430FX chipset.
CPU Addr. Pipelining	Pipelining allows the system controller to signal the CPU for a new memory address even before all data transfers for the current cycle are complete, resulting in increased throughput.
CPU Burst Write Assembly	The chipset maintains four posted write buffers. When this option is enabled, the chipset is allowed to assemble long PCI bursts from the data held in these buffers.

CPU Core Voltage	Set this field to match the voltage of the installed CPU, or set to Auto to permit the BIOS to autodetect the voltage. End users should not change the value in this field unless they replace the CPU with one of a different voltage. VP2
CPU fan on temp high	When the CPU temperature reaches a preset limit, the CPU fan turns on.
CPU Host/PCI Clock	Select Default or select a timing combination for the CPU and the PCI bus. When set to Default, the BIOS uses the actual CPU and PCI bus clock values.
CPU Internal Cache /External Cache	Cache memory is additional memory that is much faster than conventional DRAM (system memory). CPUs from 486-type on up contain internal cache memory, and most, but not all, modern PCs have additional (external) cache memory. When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU.
CPU Line Read	This field lets you Enable or Disable full CPU line reads.
CPU L2 Cache ECC Checking	When you select Enabled, memory checking is enable when the external cache contains ECC SRAMs.
CPU Line Read Multiple	A line read means that the CPU is reading a full cache line. When a cache line is full it holds 32 bytes (eight DWORDS) of data. Because the line is full, the system knows exactly how much data it will be reading and it doesn't need to wait for an end-of-data signal, freeing it to do other things. When this item is Enabled, the system is allowed to read more than one full cache line at a time.
CPU Line Read Prefetch	See the field below. When this item is Enabled, the system is allowed to prefetch the next read instruction and initiate the next process.
CPU Read Multiple Prefetch	A prefetch occurs during a process (e.g., reading from the PCI or memory) when the chipset "peeks" at the next instruction and actually begins the next read instruction. This chipset has four read lines. A multiple prefetch means that the chipset has the capacity to initiate more than one prefetch during a process.
CPU to DRAM Page Mode	When Disabled, the memory controller closes the DRAM page after a DRAM access. When Enabled, the DRAM page remains open until the next access.

CPU to PCI Buffer	When this field is Enabled, writes from the CPU to the PCI bus are buffered, to compensate for the speed differences between the CPU and the PCI bus. When Disabled, the writes are not buffered and the CPU must wait until the write is complete before starting another write cycle.
CPU-To-PCI Burst Mem. WR.	When this option is enabled, the chipset is allowed to assemble long PCI bursts from the data held in its buffers. SIS5597
CPU to PCI Byte Merge	Byte merging permits merging of the data in consecutive CPU-to-PCI byte/word writes with the same dword address, into the same posted write buffer location. The merged collection of bytes is then sent over the PCI Bus as a single dword. Byte merging is performed in the compatible VGA range only (0A0000-0BFFFF).
CPU-To-PCI IDE Posting	Select Enabled to post write cycles from the CPU to the PCI IDE interface. IDE accesses are posted in the CPU to PCI buffers, for cycle optimization.
CPU to PCI POST/BURST	Data from the CPU to the PCI bus can be posted (buffered by the controller) and/or burst. These are the methods: POST/CON.BURST Posting and conservative bursting POST/Agg.BURST Posting and aggressive bursting NONE/NONE Neither posting nor bursting POST/NONE Posting but not bursting
CPU-To-PCI Write Buffer	When Enabled, the CPU can write up to four dwords of data to the PCI write buffer before the CPU must wait for the PCI bus cycles to finish. When Disabled, the CPU must wait after each write cycle until the PCI bus signals that it is ready to receive more data.
CPU-To-PCI Write Post	When this field is Enabled, writes from the CPU to the PCI bus are buffered, to compensate for the speed differences between the CPU and the PCI bus. When Disabled, the writes are not buffered and the CPU must wait until the write is complete before starting another write cycle.
CPU Warning Temperature	Select the combination of lower and upper limits for the CPU temperature. If the CPU temperature extends beyond either limit, any warning mechanism programmed into your system will be activated.
CPU/PCI Write Phase	Determines the number of clock signals between the address and data phases of the CPU-master-to-PCI-slave writes.

CPUFAN Off in Suspend	When Enabled, the CPU fan turns off during Suspend mode.
CRT Power Down	When Enabled, the CRT powers down when the system enters a Green mode.
CRT Sleep	Determines the manner in which the monitor is blanked.
Current CPU Temperature	This field displays the current CPU temperature, if your computer contains a monitoring system.
Current CPUFAN 1/2/3 Speed	These fields display the current speed of up to three CPU fans, if your computer contains a monitoring system.
Current System Temperature	This field displays the current system temperature, if your computer contains a monitoring system.
D	
Date	The BIOS determines the day of the week from the other date information; this field is for information only. Press the right or left arrow key to move to the desired field (date, month, year). Press the PgUp or PgDn key to increment the setting, or type the desired value into the field.
Day of Month Alarm	Select a date in the month. Select 0 (zero) if you prefer to set a weekly alarm. SIS5597
Daylight Saving	When enabled, this parameter adds one hour to the clock when daylight-saving time begins. It also subtracts one hour when standard time returns.
Delayed Transaction	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specification version 2.1.
Dirty pin selection	When Combine is selected in the Tag/Dirty Implement field, you can choose whether the dirty data pin is I/O, for bi-directional input/output, or IN, for input only.
DMA Clock	This item allows you to set the speed of Direct Memory Access (DMA) at either equal to or one-half of the SYSCLK (system clock signal) speed. While speed is always desirable, choosing the higher setting may prove to be too fast for some components.
DMA *n* Assigned to	When resources are controlled manually, assign each system DMA channel as one of the following types: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific DMA channel

	PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.
Doze Mode	After the selected period of system inactivity, the CPU clock runs at slower speed while all other devices still operate at full speed.
Doze Speed (div by)	Select a divisor to reduce the CPU speed during Doze mode to a fraction of the full CPU speed.
Doze Timer	After the selected period of system inactivity, the CPU clock runs at slower speed while all other devices still operate at full speed.
Doze Timer Select	Select the timeout period (period of system inactivity) after which the system enters Doze mode.
DRAM Auto Configuration	The system board designer must select the proper value for this field, according to the specifications of the installed DRAM chips. When Disabled, you can select the DRAM timing type.
DRAM Data Integrity Mode	Select Parity or ECC (error-correcting code), according to the type of installed DRAM.
DRAM ECC/PARITY Select	Set this option according to the type of DRAM installed in your system: error-correcting code (ECC) or parity (default).
DRAM Enhanced Paging	When Enabled, the chipset keeps the page open until a page/row miss. When Disabled, the chipset uses additional information to keep the DRAM page open when the host may be "right back."
DRAM Fast Leadoff	Select Enabled to shorten the leadoff cycles and optimize performance.
DRAM Last Write to CAS#	Select the number of cycles elapse between the last data signal and CAS# asserted. This period is the setup time for the CAS signal.
DRAM Leadoff Timing	Select the combination of CPU clocks the DRAM on your board requires before each read from or write to the memory. Changing the value from the setting determined by the board designer for the installed DRAM may cause memory errors.
DRAM Page Idle Timer	Select the amount of time in HCLKs that the DRAM controller waits to close a DRAM page after the CPU becomes idle.
DRAM Page	When Disabled, the page open register is cleared and the

Open Policy	corresponding memory page is closed. When Enabled, the page remains open, even when there are no requests to service.
DRAM Posted Write	See DRAM Posted Write Buffer, next.
DRAM Posted Write Buffer	The chipset maintains its own internal buffer for DRAM writes. When this buffer is Enabled, CPU write cycles to DRAM are posted to the buffer, so the CPU can start another write cycle before the DRAM finishes its cycle.
DRAM R/W Leadoff Timing	Select the combination of CPU clocks the DRAM on your board requires before each read from or write to the memory. Changing the value from the setting determined by the board designer for the installed DRAM may cause memory errors.
DRAM RAS Only Refresh	An alternate to CAS-before-RAS refresh. Leave Disabled unless your DRAM requires this older method of refresh generation.
DRAM RAS# Precharge Time	Select the number of CPU clocks allocated for the Row Address Strobe (RAS#) signal to accumulate its charge before the DRAM is refreshed. If insufficient time is allowed, refresh may be incomplete and data lost.
DRAM RAS# Pulse Width	The system designer must select the number of CPU clock cycles allotted for the RAS pulse refresh, according to DRAM specifications.
DRAM Read Burst (B/E/F)	Set the timing for burst-mode reads from DRAM. The lower the timing numbers, the faster the system addresses memory.
DRAM Read Burst (EDO/FPM)	Sets the timing for reads from EDO (Extended Data Output) or FPM (Fast Page Mode) memory. The lower the timing numbers, the faster the system addresses memory. Selecting timing numbers lower than the installed DRAM is able to support can result in memory errors.
DRAM Read Prefetch Buffer	Each time there is a memory access request, a preprogrammed number of local bus clock signals is counted down. When the count reaches zero, if the number of filled posted write buffer slots is at or above a predetermined threshold value, the memory request priority is raised. This mechanism is used to control memory access latency.
DRAM Read Wait State	These DRAM timing numbers are the pattern of cycles the CPU uses to read data from the main memory. The system

	board designer must select the proper combination, depending on the memory size and access speed of the DRAMs. Do not reset this option from its default.
DRAM Read/Write Timing	Your system designer should select the timing that the system uses when reading from and writing to DRAM. Do not reset from the factory default value.
DRAM Read-Around-Write	DRAM optimization feature: If a memory read is addressed to a location whose latest write is being held in a buffer before being written to memory, the read is satisfied through the buffer contents, and the read is not sent to the DRAM.
DRAM Refresh Period	Select the period required to refresh the DRAMs, according to DRAM specifications.
DRAM Refresh Queue	Enabled permits queuing up to four DRAM refresh requests, so DRAM can refresh at optimal times. Disabled makes all refreshes priority requests. Installed DRAM must support this feature; most do.
DRAM Refresh Rate	Select the period required to refresh the DRAMs, according to DRAM specifications.
DRAM Refresh Stagger By	Select the number of clock ticks (0-7) between refreshing rows in the memory array. Selecting 0 refreshes all rows at once.
DRAM R/W Leadoff Timing	Select the combination of CPU clocks the DRAM on your board requires before each read from or write to the memory. Changing the value from the setting determined by the board designer for the installed DRAM may cause memory errors.
DRAM Slow Refresh	The default DRAM refresh request signal occurs every 15 µs. A 16-bit ISA bus master may activate a refresh request when it has bus ownership. Selecting a slow refresh period here specifies the timing of the refresh request signal from an ISA master.
DRAM Speculative Leadoff	A read request from the CPU to the DRAM controller includes the memory address of the desired data. When Enabled, Speculative Leadoff lets the DRAM controller pass the read command to memory slightly before it has fully decoded the address, thus speeding up the read process.
DRAM Speed Selection	The value in this field must correspond to the speed of the DRAM installed in your system. DO NOT change the default setting of this field, as determined by the system board manufacturer for the installed DRAM. This value is access

	speed, so a lower value means a faster system.
DRAM Timing	The value in this field depends on performance parameters of the installed memory chips (DRAM). Do not change the value from the factory setting unless you install new memory that has a different performance rating than the original DRAMs.
DRAM Timing Control	This allows you to determine the type of timing the system uses when reading or writing to DRAM. Selections are Fast, Fastest, Normal (default) and Slow. This field provides an alternative method of selecting DRAM timing. Again, the selected value must be set by the board designer, according to specifications of the installed DRAM and other board components. Turbo mode reduces CAS access time by 1 clock tick. VP2
DRAM to PCI RSLP	When Enabled, the chipset permits prefetching of two lines of data from system memory to the PCI bus.
DRAM Write Burst (B/E/F) DRAM Write Burst Timing	Sets the timing for burst-mode writes from DRAM. The lower the timing numbers, the faster the system addresses memory. Selecting timing numbers lower than the installed DRAM is able to support can result in memory errors.
DRAM Write Wait State	The system board designer may elect to insert a wait state into the DRAM write cycle, if necessary.
DREQ6 PIN as	This field lets the board designer invoke a software suspend routine by toggling the DREQ6 signal. Select Suspend SW only if your board has such a feature.
Drive A Drive B	Select the correct specifications for the diskette drive(s) installed in the computer. None — No diskette drive installed 360K, 5.25 in — 5-1/4 inch PC-type standard drive; 360 kilobyte capacity 1.2M, 5.25 in — 5-1/4 inch AT-type high-density drive; 1.2 megabyte capacity 720K, 3.5 in — 3-1/2 inch double-sided drive; 720 kilobyte capacity 1.44M, 3.5 in — 3-1/2 inch double-sided drive; 1.44 megabyte capacity 2.88M, 3.5 in — 3-1/2 inch double-sided drive; 2.88 megabyte capacity
Drive NA before	When Enabled, the NA signal is driven for one clock before

BRDY	the last BRDY# of every cycle for read/write hit cycles, thus generating ADS# in the next cycle after BRDY#, eliminating one dead cycle.
DRQ Detection	When Enabled, any activity on a DRQ signal line wakes up the system or resets the inactivity timer.
Duplex Select	In an infrared port mode, this field appears. Full-duplex mode permits simultaneous two-direction transmission. Half-duplex mode permits transmission in one direction only at a time. Select the value required by the IR device connected to the IR port.
E	
ECP Mode Use DMA	Select a DMA channel for the port.
EDO CASx# MA Wait State	The board designer may elect to insert one additional wait state before the assertion of the first CASx# for page hit cycles, thus allowing one additional clock of MA setup time to the CASx# for the leadoff page hit cycle. Do not change from the manufacturer's default unless you are getting memory addressing errors. This field applies only if EDO DRAM is installed in the system.
EDO Back-to-Back Timing	Select the number of timer ticks required for back-to-back accesses, according to the specifications of installed EDO DRAM. SIS5571
EDO DRAM Read Burst	Set the timing for burst-mode reads from DRAM. The lower the timing numbers, the faster the system addresses memory. This field applies only if EDO DRAM is installed in the system.
EDO DRAM Speed Selection	The value in this field must correspond to the speed of the DRAM installed in your system. DO NOT change the default setting of this field, as determined by the system board manufacturer for the installed DRAM. This value is access speed, so a lower value means a faster system. This field applies only if EDO DRAM is installed in the system.
EDO DRAM Write Burst	Set the timing for burst-mode writes from DRAM. The lower the timing numbers, the faster the system addresses memory. This field applies only if EDO DRAM is installed in the system.
EDO RASx# Wait State	The board designer may elect to insert one additional wait state before RAS# is asserted for row misses, thus allowing

	one additional MAX[13:0] setup time to RASx# assertion. This field applies only if EDO DRAM is installed in the system.
EDO RAS# Precharge Time	The precharge time is the number of cycles it takes for the RAS to accumulate its charge before DRAM refresh. If insufficient time is allowed, refresh may be incomplete and the DRAM may fail to retain data. This field applies only if EDO DRAM is installed in the system.
EDO RAS# to CAS# Delay	This field applies only if EDO DRAM is installed in the system. It lets you insert a timing delay between the CAS and RAS strobe signals, used when DRAM is written to, read from, or refreshed. Disabled gives faster performance; and Enabled gives more stable performance. EDO is short for Extended Data Output. EDO DRAM is faster than conventional DRAM if the cache controller in the system supports pipeline burst transfer mode. Unlike conventional DRAM, which only allows one byte to be read at a time, EDO DRAM can copy an entire block of memory to its internal cache. While the processor is accessing this cache, the memory can collect a new block to send.
EDO Read WS	Select the correct cycle timing combination for the system board design and EDO DRAM specifications.
Enhanced Memory Write	Select Enabled or Disabled for the Memory Write and Invalidate command on the PCI bus. This field must be Disabled if cache size is 512 KB and the tag address is 8 bits.
Enhanced Page Mode	Select Enabled or Disabled, according to DRAM specifications.
EPP Version	Select EPP port type 1.7 or 1.9.
Extended CPU-PIIX4 PHLDA#	When Enabled, the system controller adds one clock signal to the length of time the PHLDA# signal is active under two conditions: During the address phase at the beginning of a PCI read/write transaction Following the address phase of a CPU LOCK cycle When this field is Enabled, the Passive Release and Delayed

	Transaction fields should be Enabled.
Extended Read-Around-Write	When Enabled, reads can bypass writes within the 82450GX memory interface component(s), provided their addresses do not match.
External Cache	Cache memory is additional memory that is much faster than conventional DRAM (system memory). Most, but not all, modern PCs have additional (external) cache memory. When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU.
Extra AT Cycle WS	Select Enabled to insert one wait state in the standard AT bus cycle. Normally used when Legacy peripherals require additional response time.
F	
Fast AT Cycle	Select Enabled to shorten AT bus cycles by one ATCLK signal.
Fast Back-to-Back	When Enabled, consecutive write cycles targeted to the same slave become fast back-to-back on the PCI bus.
Fast DRAM Refresh	The cache DRAM controller offers two refresh modes, Normal and Hidden. In both modes, CAS takes place before RAS but the Normal mode requires a CPU cycle for each. On the other hand, a cycle is eliminated by "hiding" the CAS refresh in Hidden mode. Not only is the Hidden mode faster and more efficient, but it also allows the CPU to maintain the status of the cache even if the system goes into Suspend power-management mode.
Fast EDO Leadoff	Select Enabled only for EDO DRAMs in either a synchronous cache or a cacheless system. It causes a 1-HCLK pull-in for all read leadoff latencies for EDO DRAMs (i.e., page hits, page misses, and row misses). Select Disabled if any of the DRAM rows are populated with FPM DRAMs.
Fast EDO Path Select	When Enabled, a fast path is selected for CPU-to-DRAM read cycles for the leadoff, providing the system contains EDO DRAMs. It causes a 1-HCLK pull-in for all read leadoff latencies (i.e., page hits, page misses, and row misses).
Fast MA to RAS# Delay [CLK]	The values in this field are set by the system board designer, depending on the DRAM installed. Do not change the values in this field unless you change specifications of the installed DRAM or the installed CPU.

Fast RAS to CAS Delay	When DRAM is refreshed, both rows and columns are addressed separately. This setup item allows you to determine the timing of the transition from RAS to Column Address Strobe (CAS).
FDD Detection	When Enabled, any floppy drive activity wakes up the system or resets the inactivity timer.
Floppy 3 Mode Support	When Enabled, the BIOS supports a type of 3.5-in diskette drive that can read 720-KB, 1.2-MB, and 1.44-MB diskettes.
G	
Gate A20 Option	Gate A20 refers to the way the system addresses memory above 1 MB (extended memory). When set to Fast, the system chipset controls Gate A20. When set to Normal, a pin in the keyboard controller controls Gate A20. Setting Gate A20 to Fast improves system speed, particularly with OS/2 and Windows.
Global Standby Timer	After the selected period of inactivity for the entire system, the system enters Standby mode.
Global Suspend Timer	After the selected period of global Standby mode, the system enters Suspend mode.
GPI05 Power Up Control	When you select Enabled, a signal from General Purpose Input 05 returns the system to Full On state. SIS5597
Graphic Posted Write Buff	The chipset maintains its own internal buffer for graphics memory writes. When this buffer is Enabled, CPU write cycles to graphics memory are posted to the buffer, so the CPU can start another write cycle before the graphics memory finishes its cycle.
Guaranteed Access Time	When Enabled, Guaranteed Access Time mode is enabled, so a CHRDY time-out of 2.5 (s is guaranteed for the ISA bus. When Disabled, an ISA bus master is granted the ISA bus and then the SIO chip arbitrates for the PCI bus.
H	
Halt On	During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can tell the BIOS to ignore certain errors during POST and continue the boot-up process. These are the selections: No errors — POST does not stop for any errors. All errors — If the BIOS detects any non-fatal error, POST stops and prompts you to take corrective

		action.
	All, But Keyboard	POST does not stop for a keyboard error, but stops for all other errors.
	All, But Diskette	POST does not stop for diskette drive errors, but stops for all other errors.
	All, But Disk/Key	POST does not stop for a keyboard or disk error, but stops for all other errors.
Hard Disks	The BIOS supports up to four IDE drives. This section does not show information about other IDE devices, such as a CD-ROM drive, or about other hard drive types, such as SCSI drives. ***NOTE:*** *We recommend that you select type AUTO for all drives.* The BIOS can automatically detect the specifications and optimal operating mode of almost all IDE hard drives. When you select type AUTO for a hard drive, the BIOS detects its specifications during POST, every time the system boots. If you do not want to select drive type AUTO, other methods of selecting the drive type are available: 1. Match the specifications of your installed IDE hard drive (s) with the preprogrammed values for drive types 1 through 45. 2. Select USER and enter values into each drive parameter field. 3. Use the IDE HDD AUTO DECTECTION function in Setup. Here is a brief explanation of drive specifications: • Type: The BIOS contains a table of pre-defined drive types. Each defined drive type has a specified number of cylinders, number of heads, write precompensation factor, landing zone, and number of sectors. Drives whose specifications do not accommodate any pre-defined type are classified as type USER. • Size: Disk drive capacity (approximate). Note that this size is usually slightly greater than the size of a formatted disk given by a disk-checking program.	

	• Cyls: Number of cylinders • Head: Number of heads • Precomp: Write precompensation cylinder • Landz: Landing zone • Sector: Number of sectors • Mode: Auto, Normal, large, or LBA o Auto: The BIOS automatically determines the optimal mode. o Normal: Maximum number of cylinders, heads, and sectors supported are 1024, 16, and 63. o Large: For drives that do not support LBA and have more than 1024 cylinders. Applicable to only a few drives. o LBA (Logical Block Addressing): During drive accesses, the IDE controller transforms the data address described by sector, head, and cylinder number into a physical block address, significantly improving data transfer rates. For drives with greater than 1024 cylinders.
HDD Detection	When Enabled, any hard drive activity wakes up the system or resets the inactivity timer.
HDD Off After	After the selected period of drive inactivity, the hard disk drive powers down while all other devices remain active. Selecting Suspend tells the drive to power down immediately.
HDD Power Down	After the selected period of drive inactivity, the hard disk drive powers down while all other devices remain active.
HDD Standby Timer	After the selected period of drive inactivity, the hard disk drive powers down. Its timing is separate from other PM modes listed above.
Hidden Refresh	When Disabled, DRAM is refreshed by IBM AT methodology, using a CPU cycles for each refresh. When hidden refresh is Enabled, the DRAM controller seeks the most opportune moment for a refresh, regardless of CPU cycles, with least disruption of system activity and least performance penalty. Hidden refresh is faster and more efficient, and it also allows the CPU to maintain the status of the DRAM even if the system goes into a power management "suspend" mode.
Host-to-PCI Bridge Retry	When Enabled, the peripherals controller (PIIX4) retries, without initiating a delayed transaction, CPU-initiated

	nonLOCK# PCI cycles. No delayed transactions to the controller may be currently pending and passive release must be active. When this field is Enabled, the Passive Release and Delayed Transaction fields should be Enabled.
Hot Key Power Off	Select Enabled if your system has a hot key for soft power off. SIS5597
I	
I/O Recovery Time	The peripheral controller insert a minimum of 2 bus clock (BCLK) delays between back-to-back 8- or 16-bit ISA I/O cycles issued from the PCI master. If a greater delay is desired, select 4, 8, 12 clocks.
IDE 32-bit Transfer Mode	The IDE interface in the integrated peripherals controller supports 32-bit data transfers. Select enabled only if your IDE hard drives can also support 32-bit transfer mode.
IDE Buffer for DOS & Win	Select Enabled to increase throughput to and from IDE devices by using the on-chip read-ahead and posted-write IDE buffers. Note that use of the buffers may cause some slow IDE devices to be even slower. When in doubt, experiment with this setting for optimal performance and data integrity.
IDE Burst Mode	Selecting Enabled reduces latency between each drive read/write cycle, but may cause instability in IDE subsystems that cannot support such fast performance. If you are getting disk drive errors, try setting this value to Disabled. This field does not appear when the Internal PCI/IDE field is Disabled.
IDE Data Port Post Write	Selecting Enabled speeds up processing of drive reads and writes, but may cause instability in IDE subsystems that cannot support such fast performance. If you are getting disk drive errors, try setting this value to Disabled.
IDE HDD Block Mode	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
IDE Prefetch Mode	The onboard IDE drive interfaces supports IDE prefetching, for faster drive accesses. If you install a primary and/or secondary add-in IDE interface, set this field to Disabled if the interface does not support prefetching.
IDE Primary/	The four IDE PIO (Programmed Input/Output) fields let you

Secondary Master/Slave PIO	set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.
IDE Primary/ Secondary Master/Slave UDMA	UDMA (Ultra DMA) is a DMA data transfer protocol that utilizes ATA commands and the ATA bus to allow DMA commands to transfer data at a maximum burst rate of 33 MB/s. When you select Auto in the four IDE UDMA fields (for each of up to four IDE devices that the internal PCI IDE interface supports), the system automatically determines the optimal data transfer rate for each IDE device.
IDE Second Channel Control	The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the secondary on-chip IDE interface. Select Disabled to deactivate this interface, if you install a secondary add-in IDE interface.
In Order Queue Depth	Select 8 to track up to eight pipelined bus transactions.
IN0-IN6 (V)	These fields display the current voltage of up to seven voltage input lines, if your computer contains a monitoring system.
Inactive Timer Select	Select the timeout period (period of system inactivity) after which the system enters Inactive mode. This period should be longer than the period selected for Standby mode.
Init AGP Display First Init Display First	Initialize the AGP video display before initializing any other display device on the system. Thus the AGP display becomes the primary display.
Internal PCI/IDE	The chipset contains a PCI IDE interface that supports two IDE channels: Primary (IRQ 14) and Secondary (IRQ 15). Each channel supports two IDE devices, so the system is capable of supporting a total of four IDE devices. Select Primary, Secondary, or Both to activate chipset IDE interface (s) installed on your system board.
InfraRed Duplex Type IR Function Duplex	Select the value required by the IR device connected to the IR port. Full-duplex mode permits simultaneous two-direction transmission. Half-duplex mode permits transmission in one direction only at a time. If no infrared port is present in the system, select Disabled.
IR Duplex Mode	Select the value required by the IR device connected to the

	IR port. Full-duplex mode permits simultaneous two-direction transmission. Half-duplex mode permits transmission in one direction only at a time. If no infrared port is present in the system, select Disabled.
IRQ n Assigned to	When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1) PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.
IRQ8 Break Suspend IRQ8 Break [Event From] Suspend	You can Enable or Disable monitoring of IRQ8 (the Real Time Clock) so it does not awaken the system from Suspend mode.
IRQ8 Clock Event..	You can turn On or Off monitoring of IRQ8 (the Real Time Clock) so it does not awaken the system from Suspend mode.
IRQn Detection	When Enabled, any activity from the selected IRQ (IRQ3-IRQ12; IRQ14-IRQ15) wakes up the system or resets the inactivity timer.
IRRX Mode Select	This field appears only when IrDA mode 1.1 is selected for UART2 Mode. The value in this field depends on the type of transceiver module used for IrDA mode 1.1 (called fast IR). One type has a mode pin (IRMODE) and the other type has a second receive data channel (IRRX3). Do not change the factory default value of this field unless your IR peripheral documentation explicitly states a mode requirement for fast IR, or if you are having a problem configuring your IR peripheral in fast IR mode.
ISA Bus Clock	You can set the speed of the AT bus at one-third or one-fourth of the CPU clock speed.
ISA Bus Clock Option ISA Bus Clock Frequency	The ISA bus clock speed is the speed at which the CPU communicates with the AT bus (expansion bus). The speed is measured as a fraction of PCICLKI, the timing signal of the PCI bus. Experiment with setting the bus timing to a lower speed (for example, from PCICLKI/3 to PCICLKI/4) if an

	installed expansion peripheral has performance problems.
ISA Clock	You can set the speed of the AT bus at one-third or one-fourth of the CPU clock speed.
ISA I/O Recovery	The CPU and local bus are much faster than industry standard architecture (ISA) input/output (I/O) bus. Select Enabled to allow additional time for I/O devices to respond to the system. Otherwise, data could be lost. If all your I/O devices are capable of fast I/O, selecting Disabled can speed up processing.
ISA Line Buffer	The PCI to ISA Bridge has an 8-byte bidirectional line buffer for ISA or DMA bus master memory reads from or writes to the PCI bus. When Enabled, an ISA or DMA bus master can prefetch two doublewords to the line buffer for a read cycle.
J	
Joystick Function	If your system has a joystick peripheral, select Enable.
K	
KBC input clock	The system designer must select the correct frequency for the keyboard controller input clock. Do not change this value from the default value.
Keyboard Controller Clock	The keyboard controller clock speed is the speed at which the CPU communicates with the keyboard controller. Depending on the specifications of the installed keyboard controller, the speed may be fixed at 7.16 MHz or may be a fraction of PCICLKI, the timing signal of the PCI bus.
Keyboard Emulation	When Enabled, Gate A20 and software reset emulation for an external keyboard controller are enabled. Be sure to make the setting of this field agree with the setting of the Gate A20 Option field in the BIOS Features Setup screen (Fast = Enabled; Normal = Disabled).
Keyboard Resume	When Disabled, keyboard activity does NOT awaken the system from Suspend mode. VP2
L	
L1 Cache Policy	Write-Through means that memory is updated with data held in the cache whenever the CPU issues a write cycle. On the other hand, Write-Back causes memory to be updated only under certain conditions, such as read requests to the memory whose contents are currently in the cache. Write-Back allows the CPU to operate with fewer interruptions,

	increasing its efficiency.
L2 Cache Cacheable Size	Select 512 MB only if your system RAM is greater than 64 MB.
L2 Cache Write Policy	In addition to the Write-Back and Write-Through options, the L2 cache also offers Adaptive WB1 and Adaptive WB2. Both adaptive write-back modes try to reduce the disadvantages of both the write-through and write-back policies. The system designer must select the optimal cache write policy, according to the SRAM specifications.
L2 to PCI Read Buffer	The chipset maintains its own internal buffer for external-cache-to-PCI writes. When this buffer is Enabled, external cache write cycles to the PCI bus are posted to the buffer, so the each device can complete its cycles without waiting for the other.
L2 (WB) Tag Bit Length	The system uses tag bits to determine the status of data in the cache. Set this field to match the specifications (7 or 8 bits) of the system external cache.
LCD&CRT	Select your video display device: LCD Notebook liquid crystal display CRT Auxiliary monitor AUTO The BIOS autosenses the device in use (this value lets you switch between devices without being left "in the dark"). LCD&CRT Display on both devices
LDEV Detection	When Enabled, any activity on the LDEV signal line wakes up the system or resets the inactivity timer.
Linear Merge	When Enabled, only consecutive linear addresses can be merged.
Linear Mode SRAM Support	Select Enabled if your system contains a CPU that requires linear mode (e.g., Cyrix M1/M2 CPU).
Local Memory 15-16M	To increase performance, your system can map slower device memory (usually a device is connected to the slower ISA bus) into much faster local bus memory. It does this by setting aside local memory and transferring the start point from the device memory to the local memory. Use this setting to enable/disable this capability. It is Enabled by default.
LREQ Detection	When Enabled, any activity on the LREQ signal line wakes up the system or resets the inactivity timer.

M	
M1 Linear Burst Mode	Select Enabled if your system contains a Cyrix M1 CPU.
MA Additional Wait State	Selecting Enabled inserts an additional wait state before the beginning of a memory read. The setting of this parameter depends on the board design. Do not change from the manufacturer's default unless you are getting memory addressing errors.
Master Mode Byte Swap Master Byte Swap Control	Select Enabled or Disabled.
Master Retry Timer	This sets how many PCI clock signals the CPU master attempts a PCI cycle before the cycle is unmasked (terminated).
Mem. Drive Str. (MA/RAS)	(Memory Address Drive Strength) This field controls the strength of the output buffers driving the MA and BA1 pins (first value) and SRASx#, SCASx#, MWEx#, and CKEx pins (second value).
Memory	You cannot change any values in the Memory fields; they are only for your information. The fields show the total installed random access memory (RAM) and amounts allocated to base memory, extended memory, and other (high) memory. RAM is counted in kilobytes (KB: approximately one thousand bytes) and megabytes (MB: approximately one million bytes). RAM is the computer's working memory, where the computer stores programs and data currently being used, so they are accessible to the CPU. Modern personal computers may contain up to 64 MB, 128 MB, or more. Base Memory — Typically 640 KB. Also called conventional memory. The DOS operating system and conventional applications use this area. Extended Memory — Above the 1-MB boundary. Early IBM personal computers could not use memory above 1 MB, but current PCs and their software can use extended memory. Other Memory — Between 640 KB and 1 MB; often called High memory. DOS may load terminate-and-stay-

	resident (TSR) programs, such as device drivers, in this area, to free as much conventional memory as possible for applications. Lines in your CONFIG.SYS file that start with LOADHIGH load programs into high memory.
Memory Hole at 15M Addr.	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
Memory Hole at 15M-16M	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
Memory Parity Check	Select Enabled if the DRAM chips in your system support parity.
Memory Parity/ECC Check	Select Enabled, Disabled, or Auto. In Auto mode, the BIOS enables memory checking automatically when it detects the presence of ECC or parity DRAM.
MODEM Use IRQ	Name the interrupt request (IRQ) line assigned to the modem (if any) on your system. Activity of the selected IRQ always awakens the system.
Monitor Event in Full On Mode	In On mode, the Standby timer (Standby Timer Select, 2-256 min) starts counting if no activity is taking place and the programmable time-out period has expired. When you Enabled monitoring (checking) of a device listed under this category, it is included in the list of devices that the system monitors during the PM timers count-down. When you Disable monitoring (checking) of a device listed under this category, activity does not interrupt the PM timers count-down.
Month Alarm	Select a month (1-12) or NA if you want the alarm active during all months. SIS5597
MPS Version Control for OS	The BIOS supports versions 1.1 and 1.4 of the Intel multiprocessor specification. Select the version supported by the operating system running on this computer.

MPU-401 Configuration	Select Enabled to configure the MPU-401 interface.
MPU-401 I/O Base Address	Select a base I/O address for the MPU-401 interface
N	
NA# Enable	Selecting Enabled permits pipelining, in which the chipset signals the CPU for a new memory address before all data transfers for the current cycle are complete, resulting in faster performance.
O	
Onboard Audio Chip	Select Enabled to use the audio capabilities of your system. Most of the following fields do not appear when this field is Disabled.
Onboard FDC/FDD Controller	Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-in FDC or the system has no floppy drive, select Disabled in this field.
Onboard IDE Controller	The chipset contains a PCI IDE interface with support for two IDE channels. Select Primary to activate the only primary IDE interface, if you install an add-in secondary interface. Select Both to activate both interfaces, or Disabled to deactivate both interfaces, if you install both a primary and a secondary add-in IDE interface.
Onboard Parallel Port	Select a logical LPT port address and corresponding interrupt for the physical parallel port.
Onboard PCI SCSI Chip	Select Enabled if your system contains a built-in PCI SCSI controller.
Onboard Serial Ports (1/2, A/B)	Select a logical COM port name and matching address for the first and second serial ports. Select an address and corresponding interrupt for the first and second serial ports.
Onboard UART 1/2	See Onboard Serial Ports, above.
Onboard UART 1/2 Mode	See UART 2 Mode. Available modes apply to selected serial port.
On-Chip IDE Controller	The integrated peripheral controller contains a IDE interface with support for two IDE channels. Select Enabled to activate the IDE interface.

On-Chip IDE First/Second Channel	The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the first and/or second IDE interface. Select Disabled to deactivate an interface, if you install a primary and/or secondary add-in IDE interface.
On-Chip Local Bus IDE	The chipset contains an enhanced IDE interface with two IDE channels. Because each channel supports two IDE devices, the system supports a total of four IDE devices. If your system board has one or two IDE connectors, this option should be Enabled. If you install an add-in IDE interface, disable one or both on-chip IDE channels.
On-Chip PCI IDE	The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the IDE interface. Select Disabled to deactivate this interface, if you install a primary and/or secondary add-in IDE interface. You can disable the second IDE interface separately in the IDE Second Channel Control field in the BIOS Features Setup screen.
On-Chip Primary/ Secondary PCI IDE	The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select Enabled to activate each channel separately.
OS Select for DRAM > 64MB	Select OS2 only if you are running OS/2 operating system with greater than 64 MB of RAM on your system.
P	
Page Hit Control	This function is used for testing the controller.
Page Mode Read WS	Select the correct cycle timing combination for the system board design and Page Mode DRAM specifications.
Parallel Port EPP Type	Select EPP port type 1.7 or 1.9, as required by your parallel peripheral.
Parallel Port Mode	Select an operating mode for the onboard parallel (printer) port. Select Normal, Compatible, or SPP unless you are certain your hardware and software both support one of the other available modes For information about parallel port modes and IEEE 1284 - 1994 Standards, visit Warp Nine Engineering.
Passive Release	When Enabled, CPU to PCI bus accesses are allowed during passive release. Otherwise, the arbiter only accepts another PCI master access to local DRAM.
PCI 2.1	Select Enabled to support compliance with PCI specification

Compliance	version 2.1.
PCI Arbitration Mode	The method by which the PCI bus determines which bus master device gains access to the bus. Typically, the system manages or arbitrates access to the PCI bus on a first-come-first-served basis. When priority is rotated, once a device gains control of the bus it is assigned the lowest priority and every other device is moved up one in the priority queue.
PCI Burst	When Enabled, data transfers on the PCI bus, where possible, make use of the high-performance PCI burst protocol, in which greater amounts of data are transferred at a single command. If the write transaction is a burst transaction, the information goes into the write buffer and burst transfers are later performed on the PCI bus. If the transaction is not a burst, PCI write occurs immediately (after a write buffer flush). VP2
PCI Burst Write Combine	When this option is Enabled, the chipset assembles long PCI bursts from the data held in these buffers.
PCI CLK	The system board designer selects whether the PCI clock is tightly synchronized with the CPU clock or is asynchronous.
PCI Delayed Transaction	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specification version 2.1.
PCI Dynamic Bursting	When Enabled, every write transaction goes to the write buffer. Burstable transactions then burst on the PCI bus and nonburstable transactions do not. VP2
PCI Fast Back to Back Wr	When Enabled, the PCI bus interprets CPU read cycles as the PCI burst protocol, so back-to-back sequential CPU memory read cycles addressed to the PCI bus will be translated into fast PCI burst memory cycles.
PCI IDE 2nd Channel	Since your chipset supports a second IDE channel, you can use this selection to enable or disable the second channel. The second channel may connect to a CD-ROM.
PCI IDE Controller	The chipset contains a PCI IDE interface that is permanently configured as the secondary IDE channel. Select Secondary to activate this IDE interface. Select Disabled to deactivate this interface, if you install an add-in secondary IDE interface.
PCI IDE IRQ Map to	This field lets you select PCI IDE IRQ mapping or PC AT (ISA) interrupts. If your system does not have one or two PCI

	IDE connectors on the system board, select values according to the type of IDE interface(s) installed in your system (PCI or ISA). Standard ISA interrupts for IDE channels are IRQ14 for primary and IRQ15 for secondary.
PCI IRQ Activated by	Leave the IRQ trigger set at Level unless the PCI device assigned to the interrupt specifies Edge-triggered interrupts.
PCI Master 0 WS Write	When Enabled, writes to the PCI bus are executed with zero wait states.
PCI Mem Line Read	When Enabled, PCI Memory Read Line commands fetch full cache lines. When Disabled, a PCI Memory Read Line command results in read partials on the CPU bus.
PCI Mem Line Read Prefetch	When Enabled, PCI Memory Commands fetch a full cache line plus a prefetch of up to three additional full cache lines. Prefetching does not cross 4-KB address boundaries. When Disabled, no line prefetching is performed for PCI Memory Read Line commands. This field is irrelevant if PCI Mem Line Read, above, is Disabled.
PCI Passive Release	When Enabled, CPU to PCI bus accesses are allowed during passive release. Otherwise, the arbiter only accepts another PCI master access to local DRAM.
PCI Posted Write Buffer	You can Enable or Disable the chipset's ability to use a buffer for posted writes initiated on the PCI bus.
PCI Preempt Timer	Set the length of time (in LCLK ticks) before one PCI master preempts another when a service request is pending.
PCI Pre-Snoop	Pre-snooping is a technique by which a PCI master can continue to burst to local memory until a 4K page boundary is reached rather than just a line boundary.
PCI Read burst WS	Select the number of cycles allotted for a PCI master burst read.
PCI Slot IDE 2nd Channel	You may separately disable the second channel on an IDE interface installed in a PCI expansion slot.
PCI Timeout	When Disabled, the PCI cycles is disconnected if the first data access is not completed with 16 PCI clocks. When Enabled, the PCI cycles remains connected, even if the first data access is not completed with 16 PCI clocks.
PCI to DRAM Buffer	Your system supports buffered writes from the PCI bus to DRAM for greater efficiency.
PCI to L2 Write	The chipset maintains its own internal buffer for PCI-to-

Buffer	external-cache writes. When this buffer is Enabled, PCI write cycles to the external cache are posted to the buffer, so the each device can complete its cycles without waiting for the other.
PCI Write Burst	When Enabled, consecutive PCI write cycles become burst cycles on the PCI bus.
PCI Write burst WS	Select the number of cycles allotted for a PCI master burst write.
PCI/VGA Palette Snoop	Leave this field at Disabled.
PCI-To-CPU Write Posting	When this field is Enabled, writes from the PCI bus to the CPU are buffered, so the PCI bus can continue writing while the CPU is occupied with other processing. When Disabled, the writes are not buffered and the PCI bus must wait until the CPU is free before starting another write cycle.
PCI-To-DRAM Pipeline	DRAM optimization feature: If Enabled, full PCI-to-DRAM write pipelining is enabled. Buffers in the chipset store data written from the PCI bus to memory. When Disabled, PCI writes to DRAM are limited to a single transfer per write cycle.
Peer Concurrency	Peer concurrency means that more than one PCI device can be active at a time.
Pipeline	Select Enabled to enable the cache pipeline function when pipelined synchronous cache SRAM is installed in the system.
Pipeline Cache Timing	For a secondary cache of one bank, select Faster. For a secondary cache of two banks, select Fastest.
Pipelined Function	When Enabled, the controller signals the CPU for a new memory address before all data transfers for the current cycles are complete, resulting in faster performance.
PM Control by APM	If Advanced Power Management (APM) is installed on your system, selecting Yes gives better power savings.
PM Events	You may disable activity monitoring of some common I/O events and interrupt requests so they do not wake up the system. The default wake-up event is keyboard activity. When On (or named, in the case of LPT & COM), any activity from one of the listed system peripheral devices or IRQs wakes up the system.

	A power-management (PM) event awakens the system from, or resets activity timers for, Suspend mode. You can disable monitoring of common interrupt requests so they do not generate PM events. VP2
PM Mode	Power management is configured for SMI Green mode, which is the mode required by the system CPU.
PM wait for APM	If Advanced Power Management (APM) is installed on your system, selecting Yes gives better power savings.
PnP BIOS Auto-Config	The Award Plug and Play BIOS can automatically configure Plug and Play-compatible devices. If you select Enabled, the Available IRQ fields disappear, because the BIOS automatically handles their configuration.
PNP OS Installed	Select Yes if the system operating environment is Plug-and-Play aware (e.g., Windows 95).
Posted PCI Memory Writes	When this field is Enabled, writes from the PCI bus to memory are posted. This is an intermediate posting. If the CPU and PCI-to-DRAM posted write buffer in enabled, the data is interleaved with CPU write data and posted a second time before being written to DRAM.
Power Button Over Ride	When you select Enabled, pressing the power button for more than 4 seconds forces the system to enter the Soft-Off state when the system has "hung." SIS5597
Power Down Activities	You may disable monitoring of common interrupt requests so they do not reset activity timers.
Power Down and Resume Events	**1** You can disable monitoring of common interrupt requests so they do not awaken the system from, or reset activity timers for, Suspend mode. **2** Select ON if you want an IRQ, when accessed, to reload the original count of the global timer. Selected IRQs also cause the system to wake up from a global Doze, Standby, or Suspend mode when accessed. The global timer is the hardware timer that counts down to Doze, Standby, and Suspend modes. If a doze timeout is set, the system enters Doze mode when the timeout expires. Then the timer reloads with the standby timeout, if one is set. If not, it reloads with the suspend timeout, if one is set. If not, the timer turns off. The timer works in a similar way for the standby and suspend timeouts. When more than one global

	timeout is set, the timeouts run one after the other.
Power Management	This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. This table describes each power management mode: Max Saving — Maximum power savings. Only Available for SL CPUs. User Define — Set each mode individually. Min Saving — Minimum power savings.
Power Up by Alarm	When you select Enabled, fields appear that let you set the alarm that returns the system to Full On state. SIS5597
Primary & Secondary IDE INT#	Each PCI peripheral connection is capable of activating up to four interrupts: INT# A, INT# B, INT# C and INT# D. By default, a PCI connection is assigned INT# A. Assigning INT# B has no meaning unless the peripheral device requires two interrupt services rather than just one. Because the PCI IDE interface in the chipset has two channels, it requires two interrupt services. The primary and secondary IDE INT# fields default to values appropriate for two PCI IDE channels, with the primary PCI IDE channel having a lower interrupt than the secondary.
Primary Frame Buffer	Select a size for the PCI frame buffer. The size of the buffer should not impinge on local memory.
PS/2 Mouse Function Control	If your system has a PS/2 mouse port and you install a serial pointing device, select Disabled.
Q	
Quick Frame Generation	When the PCI-VL bus bridge is acting as a PCI Master and receiving data from the CPU, a fast CPU-to-PCI buffer is enabled if this selection is also enabled. Using the buffer allows the CPU to complete a write even though the data has not been delivered to the PCI bus. This reduces the number of CPU cycles involved and speeds overall processing.
Quick Power On Self Test	Select Enabled to reduce the amount of time required to run the power-on self-test (POST). A quick POST skips certain steps. We recommend that you normally disable quick POST. Better to find a problem during POST than lose data during your work.
R	

RAMW# Assertion Timing	RAMW is an output signal to enable local memory writes. The system designer select Normal or Faster (by one timer tick) according to DRAM specifications.
RAS Precharge @Access End	When Enabled, RAS# remains asserted at the end of access ownership. When Disabled, RAS# is deasserted at the end of access ownership.
RAS Precharge Period RAS Precharge Time	The precharge time is the number of cycles it takes for the RAS to accumulate its charge before DRAM refresh. If insufficient time is allowed, refresh may be incomplete and the DRAM may fail to retain data.
RAS Pulse Width RAS Pulse Width Refresh	The system designer must select the number of CPU clock cycles allotted for the RAS pulse refresh, according to DRAM specifications.
RAS Timeout	When RAS timeout is Disabled, a memory refresh cycle is generated every 15 microseconds. Extra refresh cycles are generated when RAS timeout is Enabled.
RAS to CAS Delay Timing	When DRAM is refreshed, both rows and columns are addressed separately. This setup item allows you to determine the timing of the transition from RAS (row address strobe) to CAS (column address strobe).
RAS# to CAS# Address Delay	This field lets you insert a timing delay from the time RAS# is asserted to when Column Address is asserted.
RAS# to CAS# Delay	This field lets you insert a timing delay between the CAS and RAS strobe signals, used when DRAM is written to, read from, or refreshed. Disabled gives faster performance; and Enabled gives more stable performance.
Read-Around-Write	DRAM optimization feature: If a memory read is addressed to a location whose latest write is being held in a buffer before being written to memory, the read is satisfied through the buffer contents, and the read is not sent to the DRAM.
Read CAS# Pulse Width	The system designer must set the number of CPU cycles the CAS signal requires during a DRAM read operation.
Read Pipeline	You may select Enabled for this field when PBSRAMs are installed. Pipelining improves system performance. VP2
Read Prefetch Memory RD	When this item is Enabled, the system is allowed to prefetch the next read instruction and initiate the next process.
Reduce DRAM Leadoff Cycle	Selecting Enabled optimizes system DRAM performance by shortening the time required before memory read or write

	operations. The installed DRAM must support a reduced cycle.
Refresh Cycle Time (us)	Select the period required to refresh the DRAMs, according to DRAM specifications.
Refresh RAS# Assertion	Select the number of clock cycles in which RAS# is asserted for refresh cycles.
Reload Global Timer Events	When Enabled, an event occurring on each listed device restarts the global timer for Standby mode.
Report No FDD For WIN 95	Select Yes to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the Integrated Peripherals screen, select Disabled for the Onboard FDC Controller field.
Reset Configuration Data	Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.
Resources Controlled By	The Plug and Play **AwardBIOS** can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.
Resume by Ring	An input signal on the serial Ring Indicator (RI) line (in other words, an incoming call on the modem) awakens the system from a soft off state.
RTC Alarm Resume	When Enabled, your can set the date and time at which the RTC (real-time clock) alarm awakens the system from Suspend mode. VP2
S	
SDRAM Bank Interleave	Select 2 Bank or 4-Bank interleave for 64-Mb SDRAM. If 16-Mb SDRAM is installed, leave Disabled. VP2
SDRAM (CAS Lat/RAS-to-CAS)	You can select a combination of CAS latency and RAS-to-CAS delay in HCLKs of 2/2 or 3/3. The system board designer should set the values in this field, depending on the DRAM installed. Do not change the values in this field unless you change specifications of the installed DRAM or the installed CPU.
SDRAM CAS	When synchronous DRAM is installed, the number of clock

Latency SDRAM CAS Latency Time	cycles of CAS latency depends on the DRAM timing. Do not reset this field from the default value specified by the system designer.
SDRAM Cycle Length	This field sets the CAS latency timing. VP2
SDRAM Precharge Control	When Enabled, all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.
SDRAM RAS Precharge Time	If an insufficient number of cycles is allowed for the RAS to accumulate its charge before DRAM refresh, the refresh may be incomplete and the DRAM may fail to retain data. Fast gives faster performance; and Slow gives more stable performance. This field applies only when synchronous DRAM is installed in the system.
SDRAM RAS to CAS Delay	This field lets you insert a timing delay between the CAS and RAS strobe signals, used when DRAM is written to, read from, or refreshed. Fast gives faster performance; and Slow gives more stable performance. This field applies only when synchronous DRAM is installed in the system.
SDRAM Speculative Read	The chipset can "speculate" on a DRAM read address, thus reducing read latencies. The CPU issues a read request containing the data memory address. The DRAM controller receives the request. When this field is Enabled, the controller issues the read command slightly before it has finished decoding the data address.
SDRAM Wait State Control	If necessary, the system designer may insert a wait state into the memory data access cycle.
SDRAM WR Retire Rate	The system designer must select the correct timing for data transfers from the write buffer to memory, according to DRAM specifications.
Security Option	If you have set a password, select whether the password is required every time the System boots, or only when you enter Setup.
Serial Port 1/2 Interrupt	Select between the default PC AT interrupt and no interrupt for COM 1/3 and COM 2/4.
Serial Port 1/2 MIDI	MIDI (musical instrument digital interface) is a standard adopted by the electronic music industry for controlling devices, such as synthesizers and sound cards, that emit music. Select Enabled for the appropriate port if a MIDI

	device is connected to serial port 1 or serial port 2.
Shadow	Software that resides in a read-only memory (ROM) chip on a device is called firmware. The Award BIOS permits shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals, such as, for example, a SCSI adaptor. Shadowing copies firmware from ROM into system RAM, where the CPU can read it through the 16-bit or 32-bit DRAM bus. Firmware not shadowed must be read by the system through the 8-bit X-bus. Shadowing improves the performance of the system BIOS and similar ROM firmware for expansion peripherals, but it also reduces the amount of high memory (640 KB to 1 MB) available for loading device drivers, etc. Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option. Video BIOS shadows into memory area C0000-C7FFF. The remaining areas shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.
Shared VGA Memory Speed	Specify the memory speed of the DRAM allocated for video memory.
Single ALE Enable	Select Enabled to activate a single ALE signal instead of multiple ALEs during a bus conversion cycle.
Single Bit Error Report	If ECC is enabled (see the previous fields), selecting Enabled here tells the system to report an error when a correctable single-bit error occurs.
Sleep Clock	Select Stop Clock or Slow Clock during Sleep mode.
Sleep Timer	After the selected period of system inactivity, all devices except the fixed disk drive and CPU shut off.
Slot 1/2/3/4 Using INT#	Some PCI devices use interrupts to signal that they need to use the PCI bus. Other devices, notably most graphics adapters, do not need interrupt service at all. Each PCI slot

	can activate up to four interrupts, INT# A, INT# B, INT# C and INT# D. By default, a PCI slot is allowed INT# A. Assigning INT# B has no meaning unless the device in the slot requires two interrupt services rather than just one. Likewise, using INT# C can only mean the device requires three interrupts; and using INT# D, four interrupts. Selecting the default, AUTO, allows the PCI controller to automatically allocate the interrupts.
Slow Refresh Enable	If your system is equipped with slow refresh DRAMs, enabling this setting causes the refresh frequency to be reduced to one-fourth the default speed.
Soft-Off by PWR-BTTN	When Enabled, turning the system off with the on/off button places the system in a very low-power-usage state, with only enough circuitry receiving power to detect power button activity or Resume by Ring activity.
Spread Spectrum Modulated	When the system clock generator pulses, the extreme values of the pulse generate excess EMI. Enabling pulse spectrum spread modulation changes the extreme values from spikes to flat curves, thus reducing EMI. This benefit may in some cases be outweighed by problems with timing-critical devices, such as a clock-sensitive SCSI device. BX
SRAM Back-to-Back	Selecting Enabled reduces the latency between 32-bit data transfers, so data is transferred in 64-bit bursts.
SRAM Read Timing	These SRAM timing numbers are the pattern of cycles the CPU uses to read data from the cache. The system board designer must select the proper combination, depending on the cache size and access speed of the cache SRAMs. Do not reset this option from its default.
SRAM Type	The system controller supports both synchronous and asynchronous cache memory. Set this field to match the type installed in your system.
SRAM Write Timing	If necessary, you can insert a wait state in the SRAM write cycle. The system board designer must select the proper wait state number. If cache memory errors occur, try adding a wait state.
Standby Mode	After the selected period of system inactivity, the fixed disk drive and the video shut off while all other devices still operate at full speed.
Standby Speed	Select a divisor to reduce the CPU speed during Standby

(div by)	mode to a fraction of the full CPU speed.
Standby Timer Select	Select the timeout period (period of system inactivity) after which the system enters Standby mode. This period should be longer than the period selected for Doze mode.
Standby Timers	After the selected period of inactivity for each subsystem (video, hard drive, peripherals), that subsystem enters Standby mode.
Starting Point of Paging	This value controls the start timing of memory paging operations.
Suspend Mode	After the selected period of system inactivity, all devices except the CPU shut off.
Suspend Mode Option	Select the type of Suspend mode: POS Power-on suspend (the CPU and core system remain powered on in a very low-power mode) Auto After the period of inactivity selected in the Auto Suspend Timeout field, the system automatically enters STD mode. If STD mode is unavailable, the system enters STR mode. STD Save to disk STR Suspend to RAM
Suspend Option	This item lets you select a method of global system suspend. Static Suspend, sometimes called Power-on Suspend (POS), leaves the CPU powered on but stops its clock. 0V Suspend, sometimes called Save to Disk (STD) Suspend, saves the state of the entire system to disk and then powers off the system.
Sustained 3T Write	You may enable this field when pipelined burst synchronous SRAM (PBSRAM) cache memory is installed. It enables sustained three-cycle write access for PBSRAM access at 66 or 75 MHz. VP2
Swap Floppy Drive	This field is effective only in systems with two floppy drives. Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.
Switch Function	1. Select the operation of the power button, when pressed: o *Deturbo.* System slows; press a key to return to full power. o *Break.* System enters Suspend mode; press a key to return to full power.

	o *Break/Wake.* System enters Suspend mode; press the power button again to return to full power. 2. You can choose whether or not to permit your system to enter complete Suspend mode. Suspend mode offers greater power savings, with a correspondingly longer awakening period. SIS5597
SYNC SRAM Support	If synchronous cache memory is installed, this setting allows you to specify whether this memory is the Standard synchronous SRAM or Pipelined SRAM.
Synchronous AT Clock	The AT bus synchronous clock speed is the speed at which the CPU communicates with the AT bus (expansion bus). The speed is measured as a fraction of CLK, the timing signal of the CPU bus. Experiment with setting the bus timing to a lower speed (for example, from CLK/3 to CLK/4) if an installed expansion peripheral has performance problems.
System BIOS Cacheable	Selecting Enabled allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may result.
T	
Tag Compare Wait States	The tag sample point can be in the first T2 cycle (0 wait states) or second T2 cycle (1 wait state). Tag operation in 0 wait states requires 12-ns SRAM or faster.
Tag Option	Select a 7-bit cache tag RAM with one dirty bit, or an 8-bit tag.
Tag RAM Size	The system uses tag bits to determine the status of data in the cache. Set this field to match the specifications (7 or 8 bits) of the installed tag RAM chip.
Tag/Dirty implement	The system cache controller supports two methods of determining the state of data in the cache. Separate separates the tag signal from the "dirty" signal while Combine combines the two in a single 8- (if 7 bits are selected above) or 9-bit (8 bits selected) signal.
Throttle Duty Cycle	When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percent of time that the clock runs.
Time	The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the right or left arrow key to move to the desired field . Press the PgUp or PgDn

	key to increment the setting, or type the desired value into the field.
Time ; Timer	Set the time you want the alarm to go off on the days when it is activated. SIS5597
Turbo Read Leadoff	Select Enabled to shorten the leadoff cycles and optimize performance in cacheless, 50-60 MHz, or one-bank EDO DRAM systems.
Turbo VGA (0 WS at A/B)	When Enabled, the VGA memory range of A_0000 to B_0000 uses a special set of performance features. This features has little or no effect during video modes beyond standard VGA, modes most commonly used for high resolution, high color displays associated with Windows, OS/2, UNIX, etc. On the other hand, this memory range is heavily used by games such DOOM.
Turn-Around Insertion	When Enabled, the chipset inserts one extra clock to the turn-around of back-to-back DRAM cycles.
TxD, RxD Active	Consult your IR peripheral documentation to select the correct setting of the TxD and RxD signals.
Typematic Delay (Msec)	When the typematic rate setting is enabled, you can select a typematic delay (the delay before key strokes begin to repeat) of 250, 500, 750 or 1000 milliseconds.
Typematic Rate (Chars/Sec)	When the typematic rate setting is enabled, you can select a typematic rate (the rate at which character repeats when you hold down a key) of 6, 8, 10,12, 15, 20, 24 or 30 characters per second.
Typematic Rate Setting	When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and typematic delay.
U	
UART 1/2 Duplex Mode	In an infrared port mode, this field appears. Full-duplex mode permits simultaneous two-direction transmission. Half-duplex mode permits transmission in one direction only at a time. Select the value required by the IR device connected to the IR port.
UART 2 Mode	Select an operating mode for the second serial port: Normal RS-232C serial port

	Standard RS-232C serial port IrDA 1.0 Infrared port compliant with IrDA 1.0 specification IrDA SIR IrDA MIR IrDA-compliant serial infrared port IrDA FIR 1 MB/sec infrared port FIR Fast Infrared standard MIR 0.57M Fast Infrared standard MIR 1.15M 0.57-MB/sec infrared port Sharp IR 1.15-MB/sec infrared port HPSIR 4-Mb/s data transmission ASK IR IrDA-compliant serial infrared port Amplitude shift keyed infrared port
UltraDMA (UDMA)	See IDE UDMA etc.
UR2 Mode	See UART2 Mode, above.
USB Controller	Select Enabled if your system contains a Universal Serial Bus (USB) controller and you have USB peripherals.
USB Keyboard Support	Select Enabled if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard.
USB Latency Time (PCI CLK)	Select the minimum amount of time, in PCI clock cycles, that the USB controller can retain ownership of the PCI bus.
Use IR Pins	Consult your IR peripheral documentation to select the correct setting of the TxD and RxD signals.
Used Mem base addr	Select a base address for the memory area used by any peripheral that requires high memory.
Used Mem Length	Select a length for the memory area specified in the previous field. This field does not appear if no base address is specified.
USWC Write Post	When video memory cache is configured for USWC mode, select Enabled for write-back cache mode.
V	
VGA Active Monitor	When Enabled, any video activity restarts the global timer for Standby mode.
VGA Frame Buffer	When Enabled, a fixed VGA frame buffer from A000h to BFFFh and a CPU-to-PCI write buffer are implemented.
VGA Memory Clock (MHz)	Set the speed (MHz) of the VGA memory clock.

VGA Performance Mode	If Enabled, the VGA memory range of A_0000 to B_0000 uses a special set of performance features. This features has little or no effect during video modes beyond standard VGA, modes most commonly used for high resolution, high color displays associated with Windows, OS/2, UNIX, etc. On the other hand, this memory range is heavily used by games such DOOM.
VGA Shared Memory Size	Specify the size of system memory to allocate for video memory, from 512 KB to 4 MB.
Video	Select the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically. The BIOS supports a secondary video subsystem, but you do not select it in Setup. EGA/VGA Enhanced Graphics Adapter/Video Graphics Array. For EGA, VGA, SEGA, SVGA or PGA monitor adapters. CGA 40 Color Graphics Adapter, power up in 40 column mode CGA 80 Color Graphics Adapter, power up in 80 column mode MONO Monochrome adapter, includes high resolution monochrome adapters
Video BIOS Cacheable	Selecting Enabled allows caching of the video BIOS ROM at C0000h to C7FFFh, resulting in better video performance. However, if any program writes to this memory area, a system error may result.
Video Buffer Cacheable	When Enabled, the video BIOS (at address C0000h to C7FFFh) is cached.
Video Detection	When Enabled, any video activity wakes up the system or resets the inactivity timer.
Video Memory Cache Mode	Select UC (uncacheable) or USWC (uncacheable, speculative write combine) mode. USWC may give better performance in accessing the video RAM buffer.
Video Off After	As the system moves from lesser to greater power-saving modes, select the mode in which you want the monitor to blank.
Video Off Method	Determines the manner in which the monitor is blanked. V/H SYNC+Blank System turns off vertical and horizontal synchronization ports and writes blanks to the

	video buffer. DPMS Support — Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values. Blank Screen — System only writes blanks to the video buffer.
Video Off Option	Selects the power-saving modes during which the monitor goes blank: Always On — Monitor remains on during power-saving modes. Suspend -- Off — Monitor blanked when system enters Suspend mode. Susp, Stby -- Off — Monitor blanked when system enters either Suspend or Standby mode. All Modes -- Off — Monitor blanked when system enters any power saving mode.
Video RAM Cacheable	Selecting Enabled allows caching of the video memory (RAM) at A0000h to AFFFFh, resulting in better video performance. However, if any program writes to this memory area, a memory access error may result.
Virus Warning	When enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive. ***NOTE:*** *Many disk diagnostic programs that access the boot sector table can trigger the virus warning message. If you plan to run such a program, we recommend that you first disable the virus warning.*
W	
Wake Up Event in Inactive Mode	Enable the interrupts that you want to awaken the system from a reduced-power mode. Disable the interrupts that you do not want to awaken the system from a reduced-power mode.
Wake Up Events	You can turn On or Off monitoring of commonly used interrupt requests so they do not awaken the system from, or

	reset activity timers for, Doze and Standby modes. For example, if you have a modem on IRQ3, you can turn On IRQ3 as a wake-up event, so an interrupt from the modem can wake up the system. Or you may wish to turn Off IRQ12 (the PS/2) mouse as a wake-up event, so accidentally brushing the mouse does not awaken the system. The default wake-up event is keyboard activity.
Watch Dog Timer	You can enable the system watch-dog timer, a hardware timer that generates either an NMI or a reset when the software that it monitors does not respond as expected each time the watch dog polls it (select the time period in a separate field). See the WDT fields, below. SIS5582
WAVE2 DMA Select	Select a DMA channel for the WAVE2 device
WAVE2 IRQ Select	Select an interrupt for the WAVE2 device.
WDT Active Time	Select the watch-dog timer period. SIS5582
WDT Configuration Port	Select the I/O port for the watch-dog timer. SIS5582
WDT Time Out Active For	Select the watch-dog timer response. SIS5582
Week Alarm	Turn the alarm On and Off on specific days. SIS5597
Word Merge	This field controls the word-merge feature for frame buffer cycles. When Enabled, the controller checks the eight CPU Byte Enable signals to determine if data words read from the PCI bus by the CPU can be merged.
Write CAS# Pulse Width	The system designer must set the number of CPU cycles the CAS signal remains asserted during a DRAM write operation.
Write Pipeline	You may select Enabled for this field when PBSRAMs are installed. Pipelining improves system performance. VP2
XYZ	
ZZ Active in Suspend	When Enabled, the ZZ signal is active during Suspend mode.

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